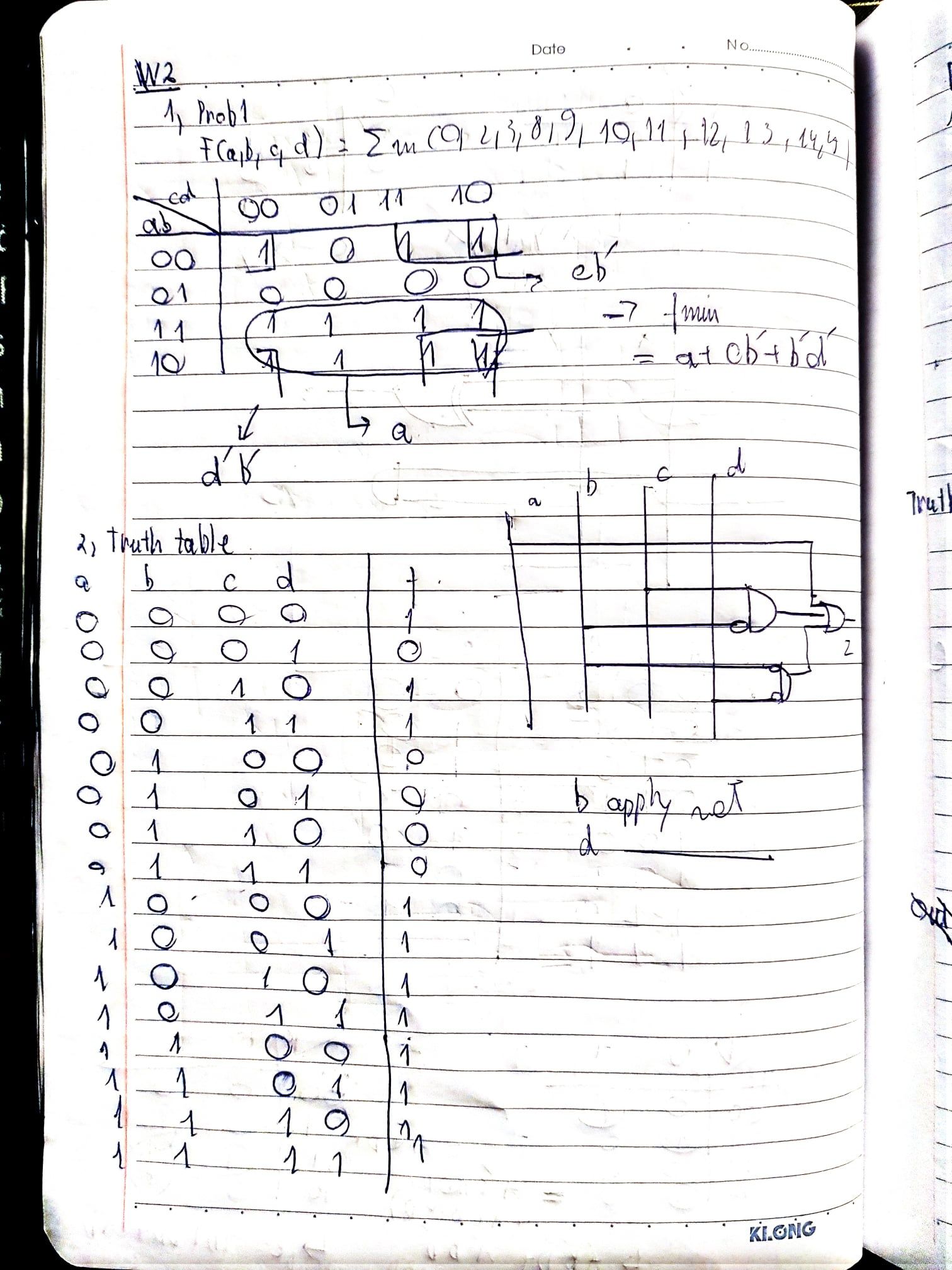
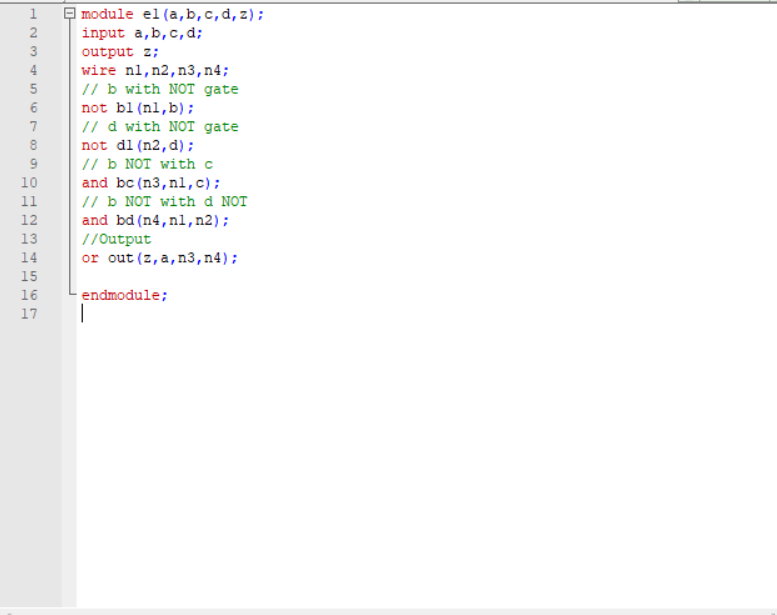
Week 2 Exercise – Dang Tran Nhat Minh – 20193231

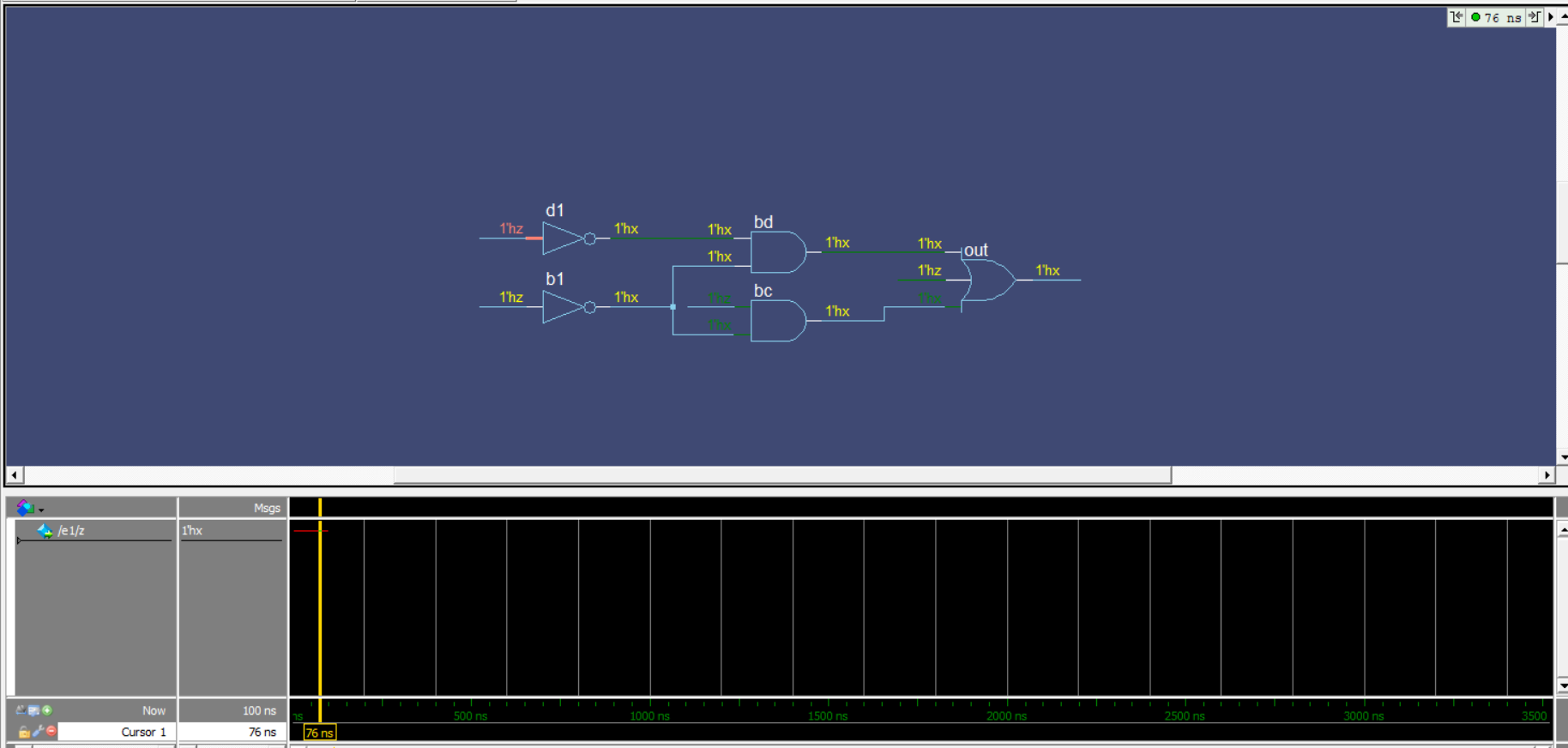
Ex1:

**K-map**



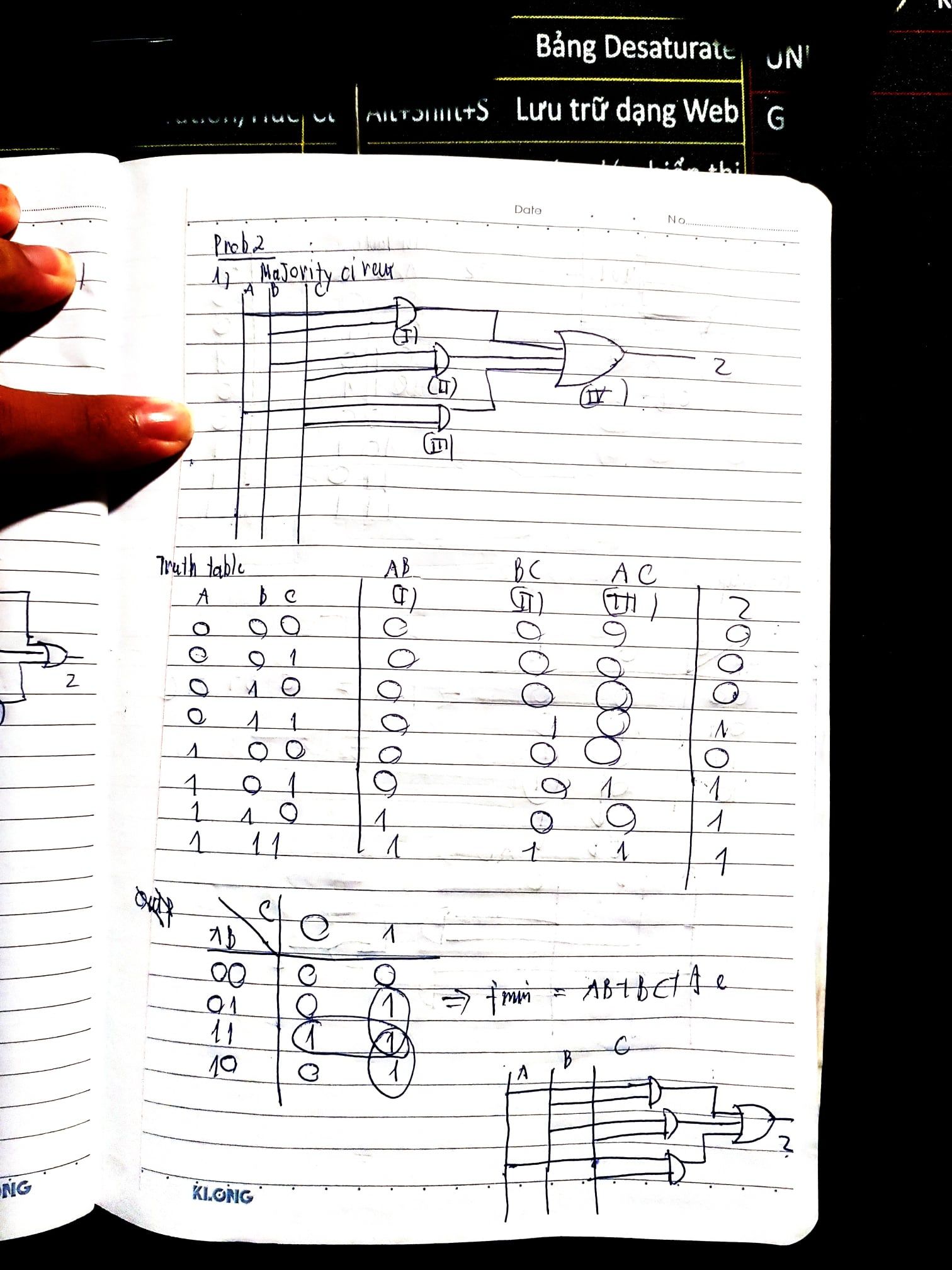
Verilog code

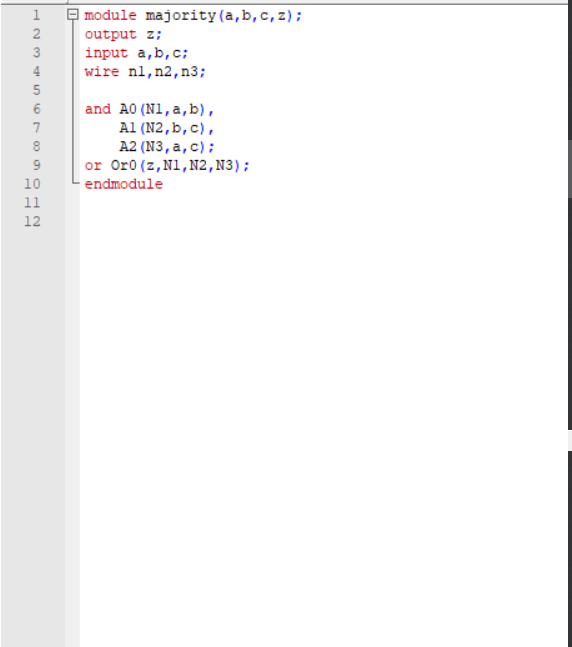


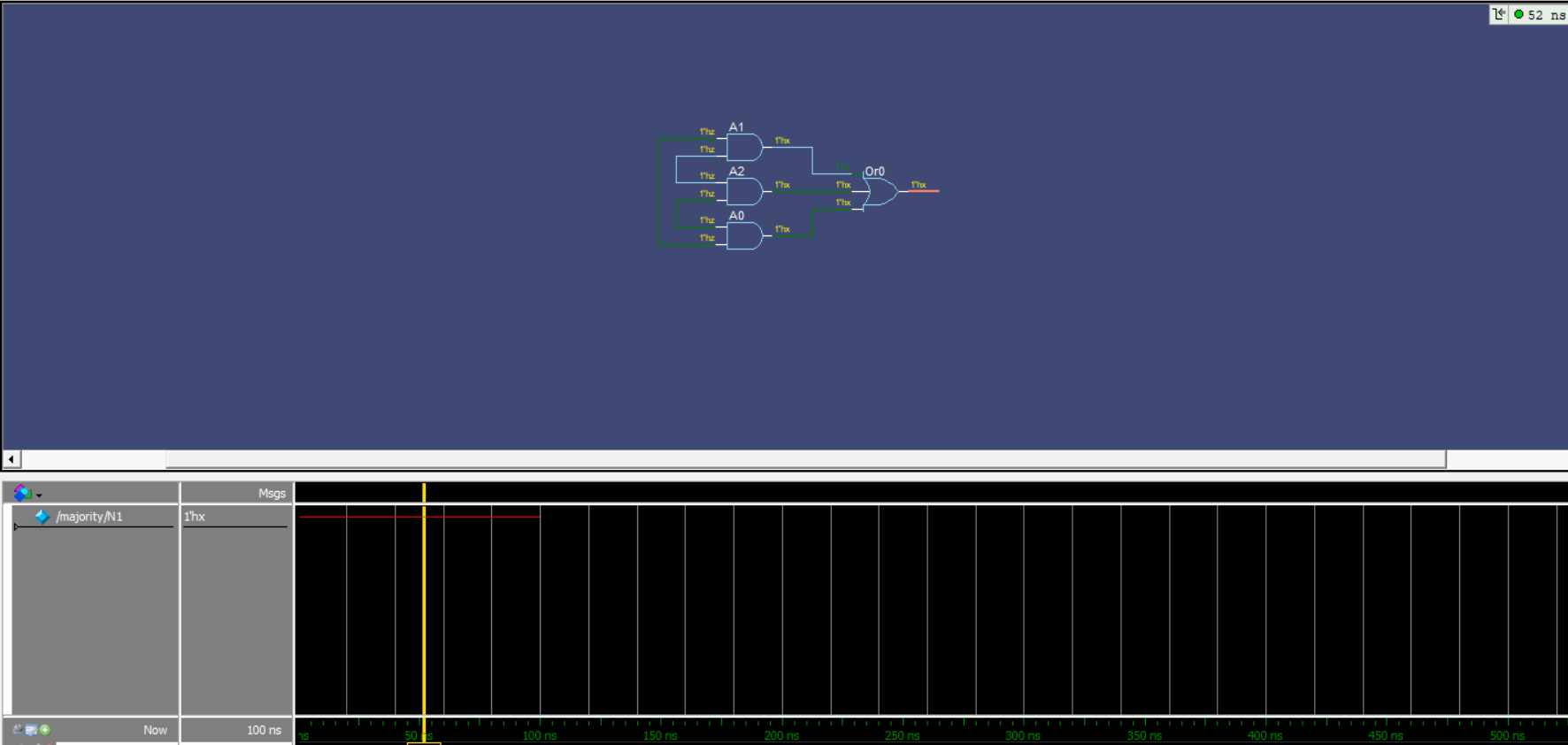


Ex2:

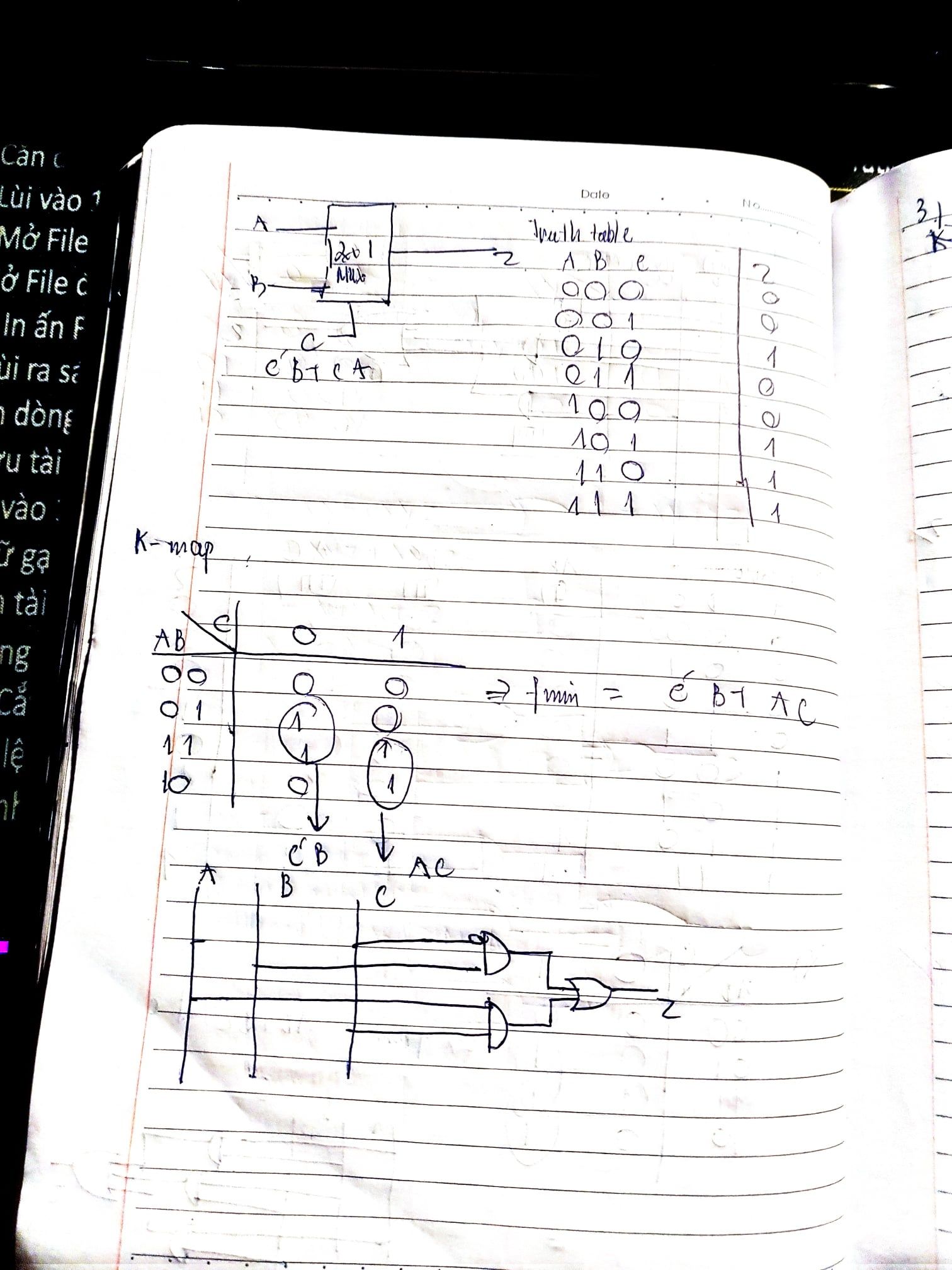
**Majority circuit**

Verilog code

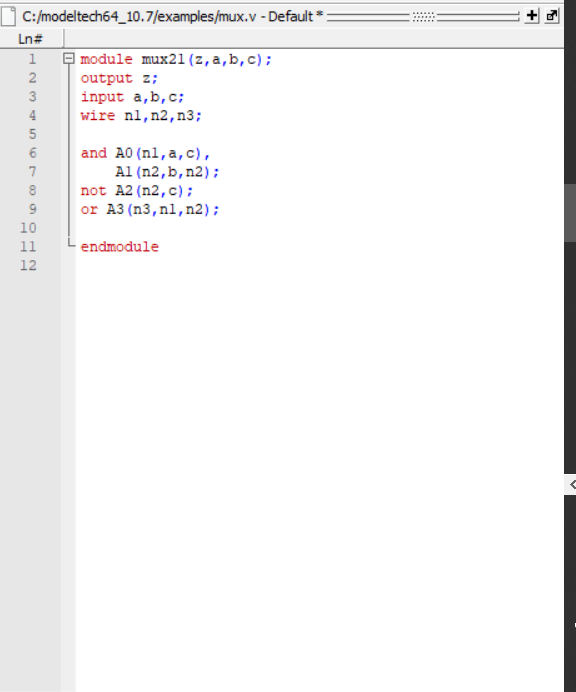


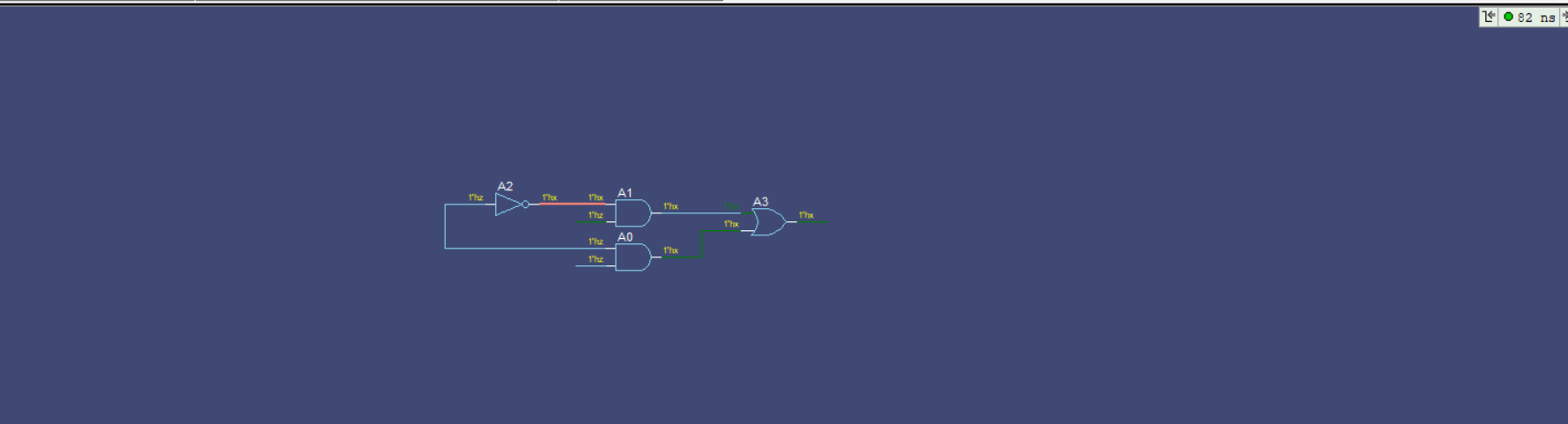


**MUX 2x1**



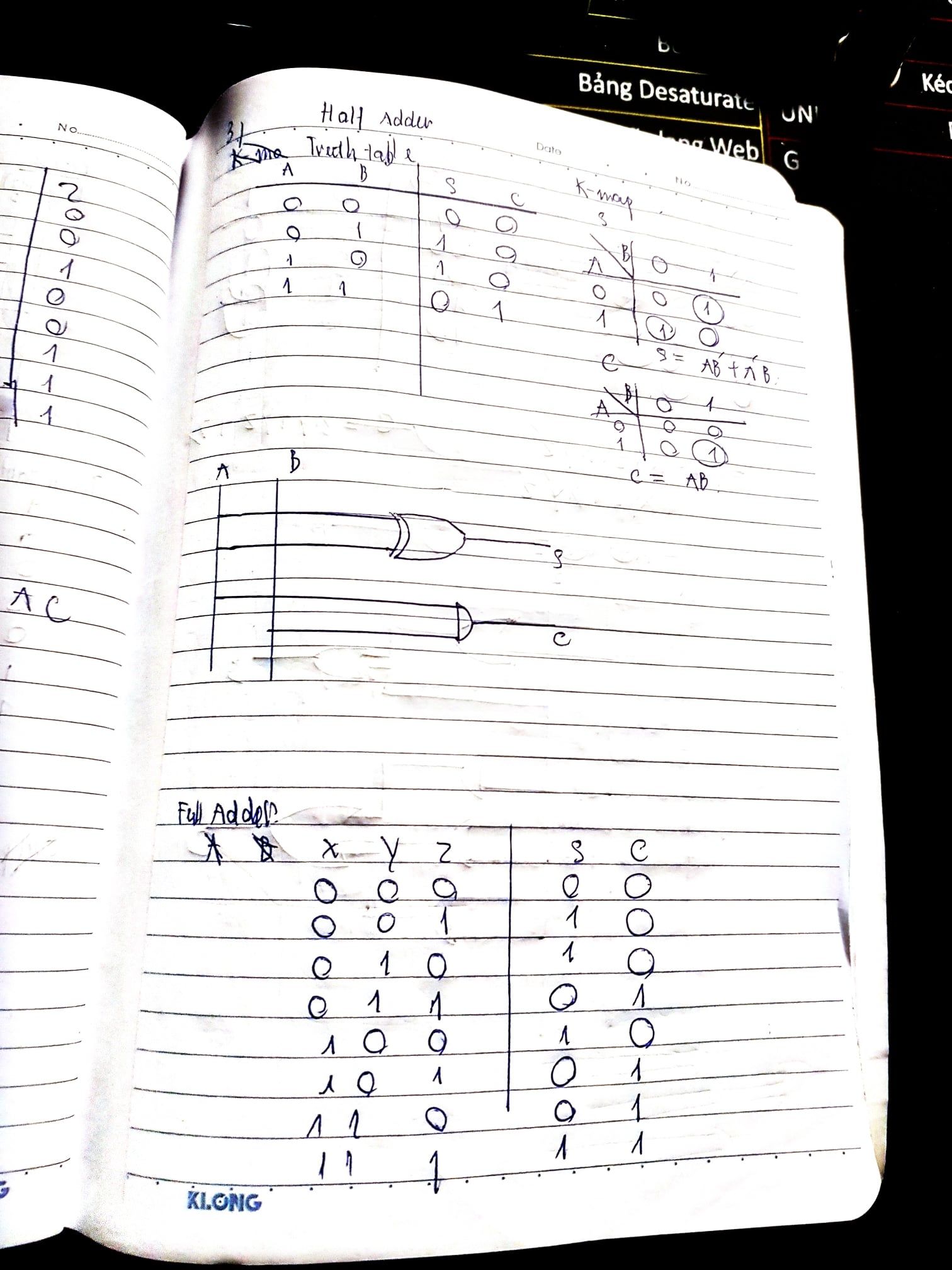
Verilog code



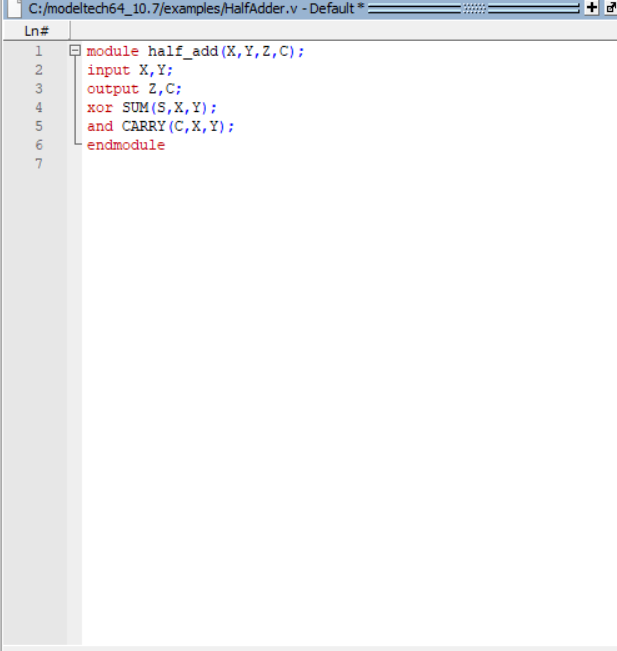


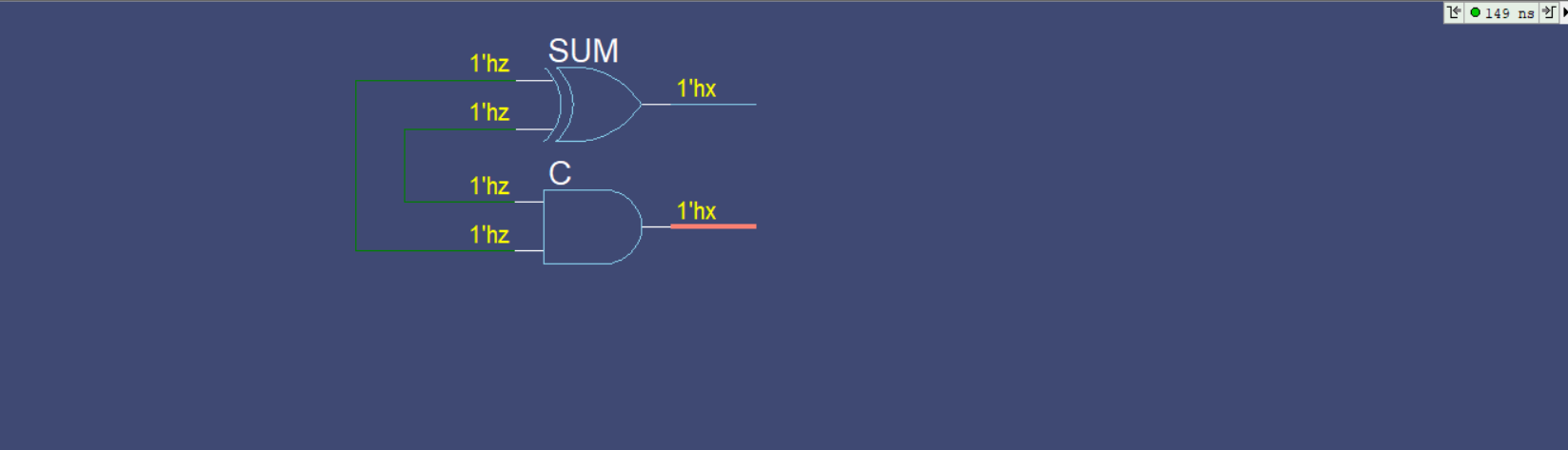
Ex 3:

**3.1 Half adder**

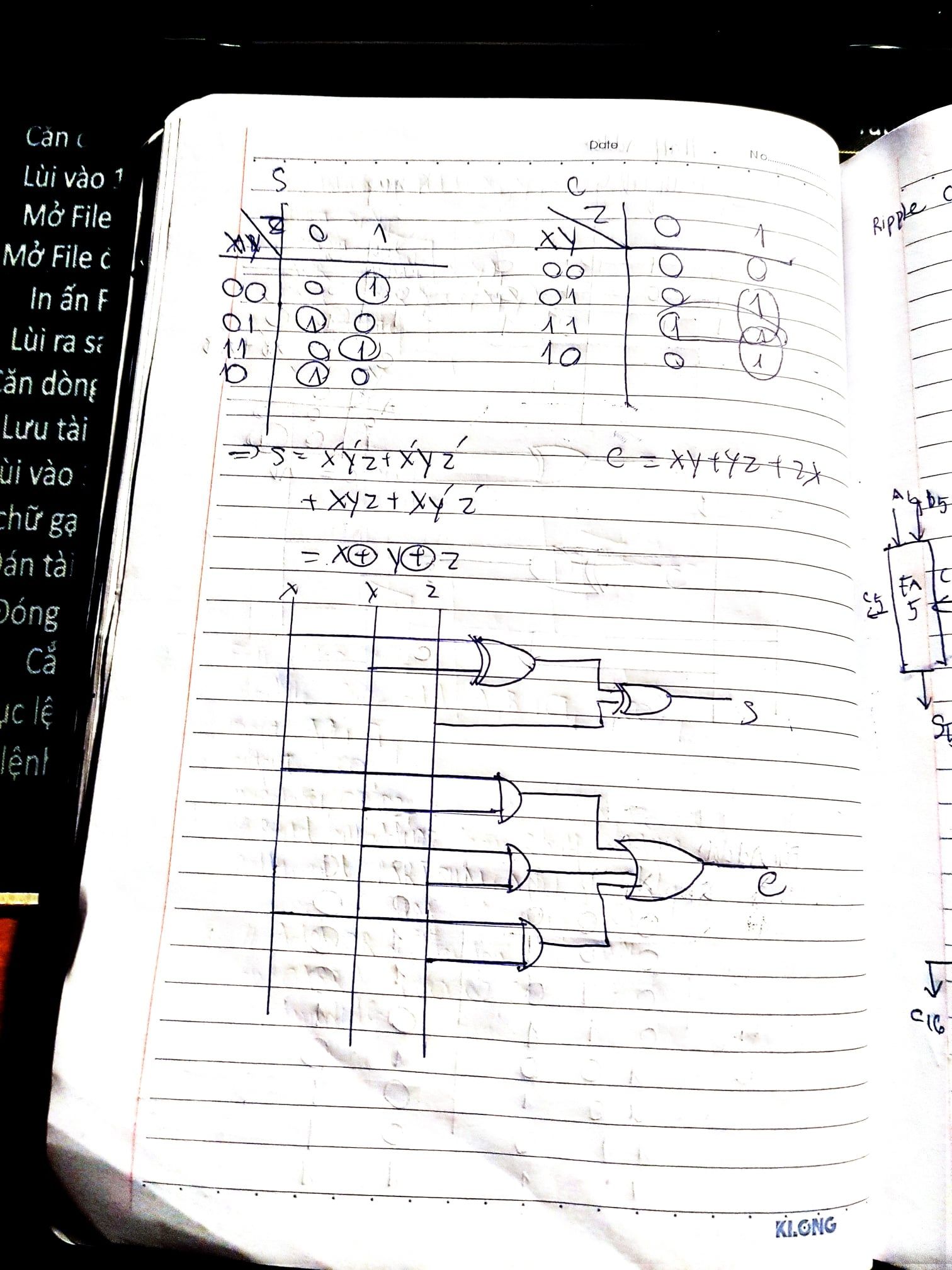


Verilog code

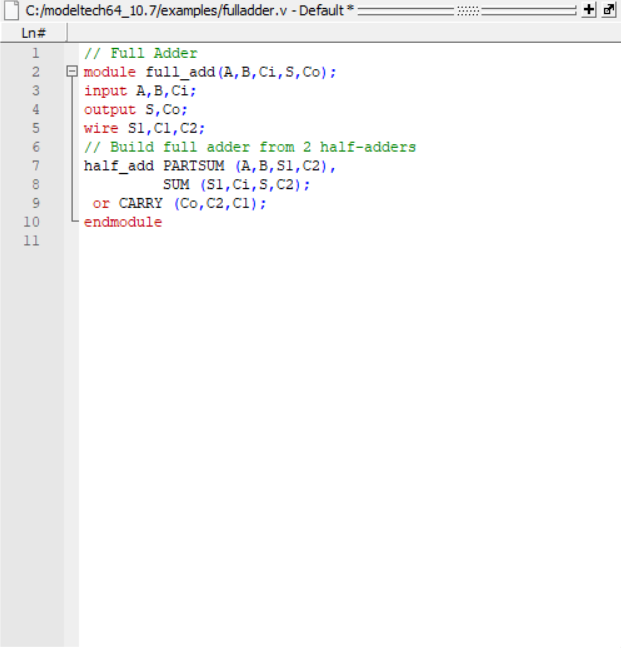


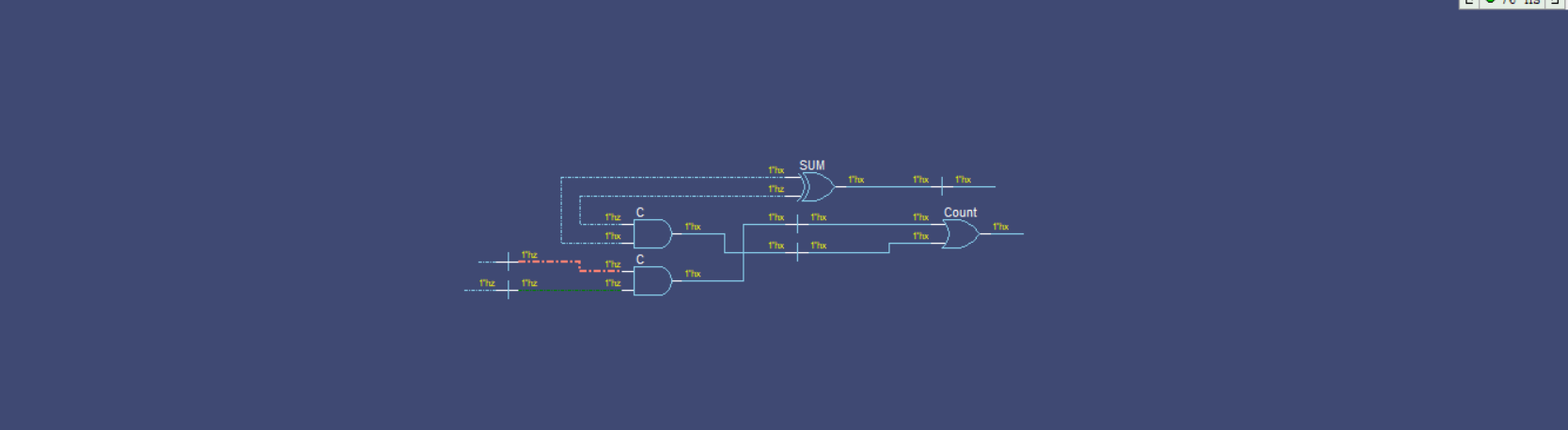


**3.2 Full adder**

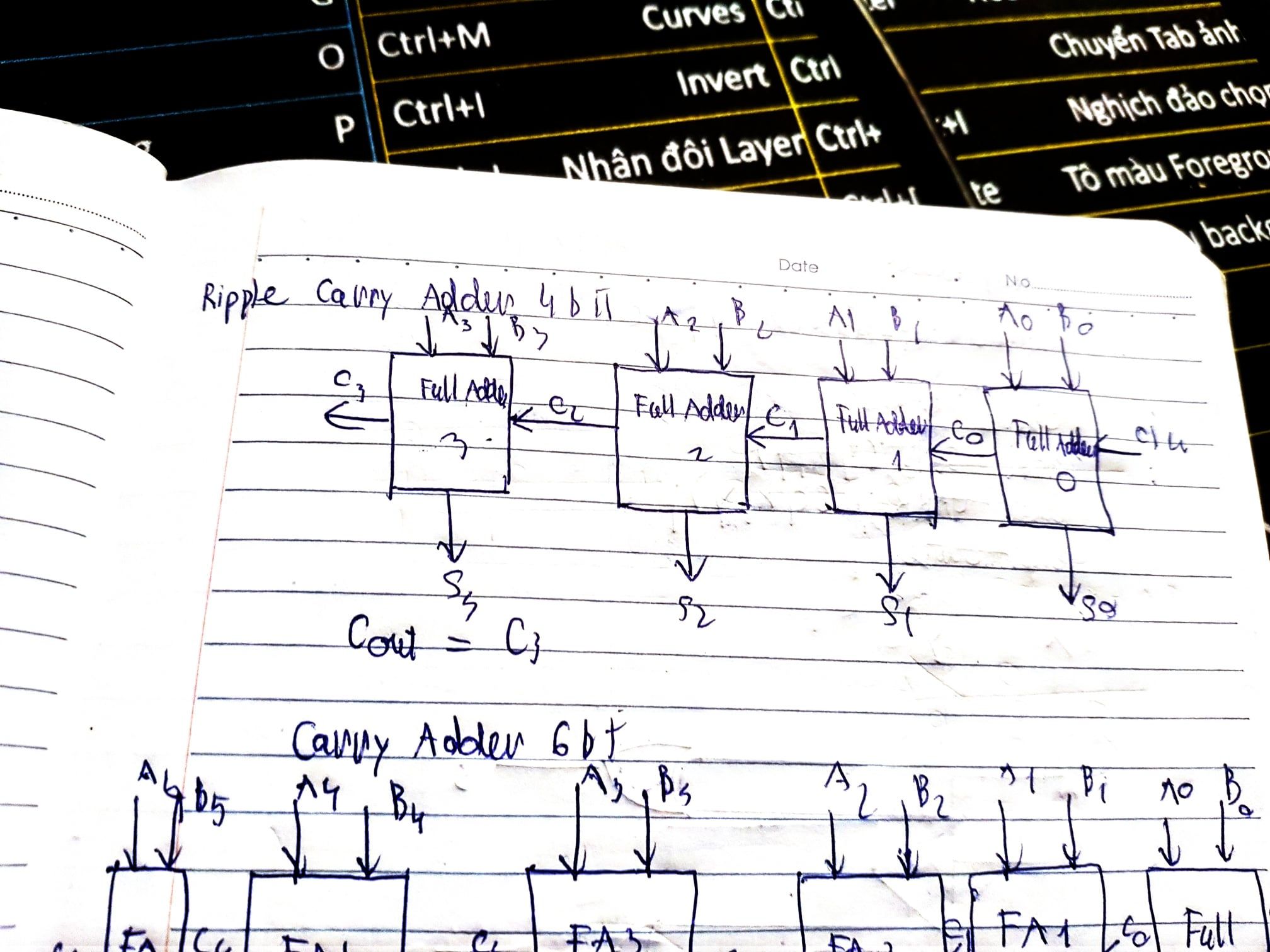


Verilog code

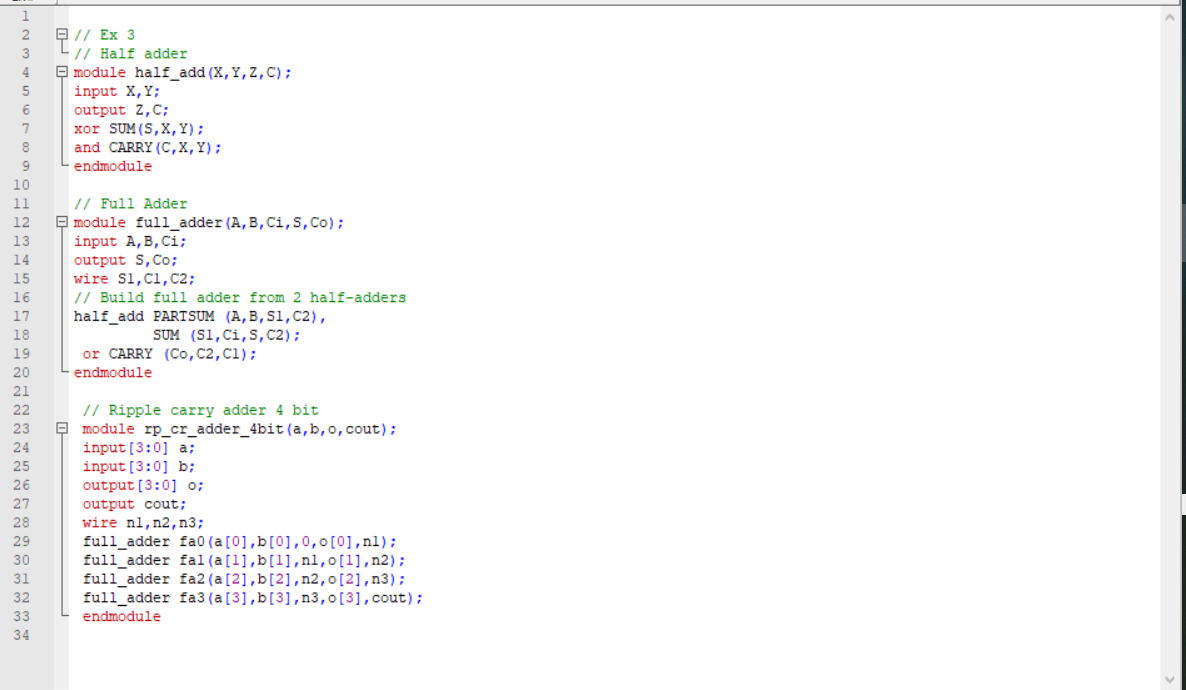




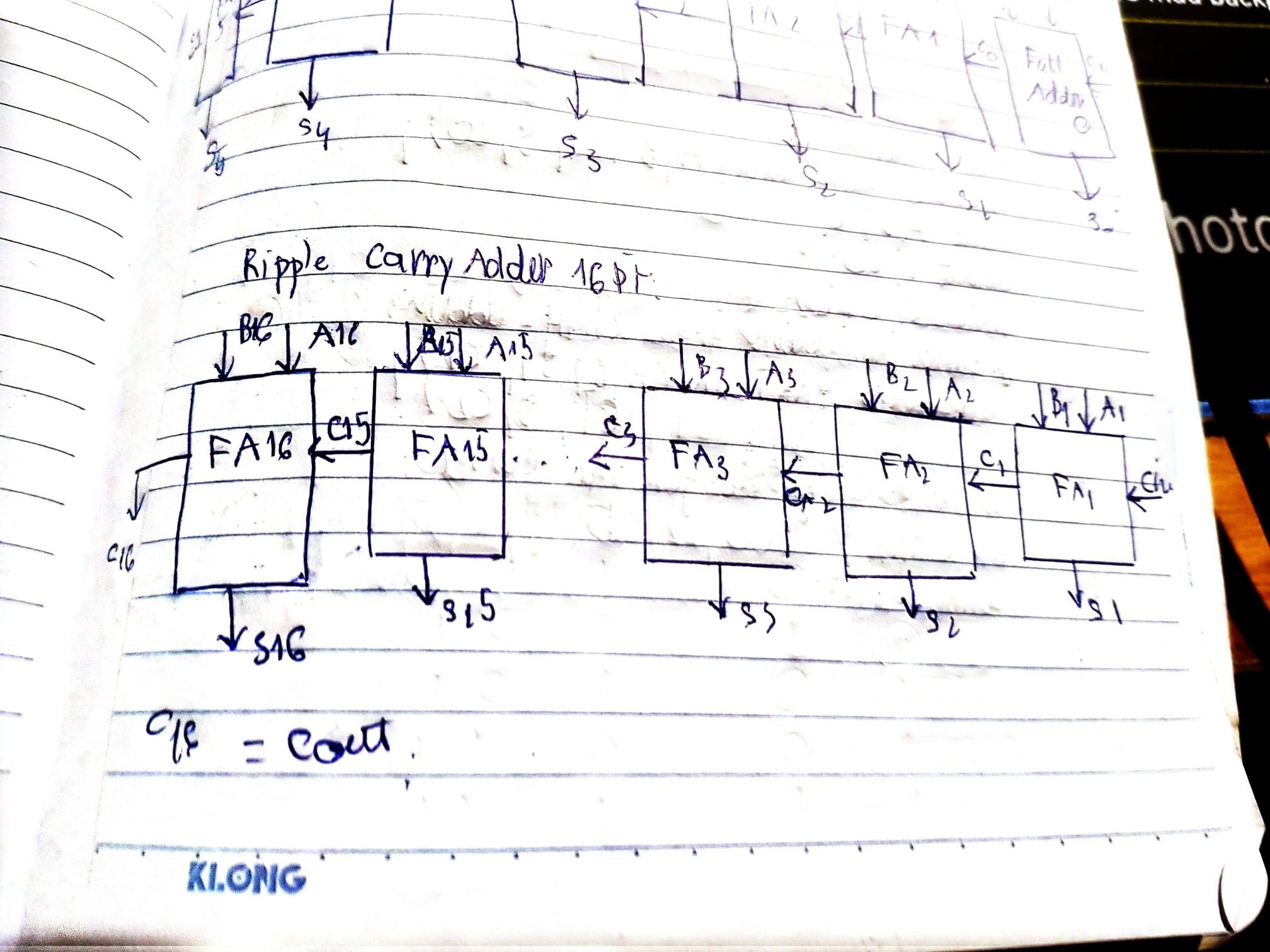
**3.3 Ripple\_Carry\_Adder\_4bit**



Verilog code



**3.4 Ripple\_carry\_adder\_16bit**



Verilog code

